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EXAMINER
NGUYEN, MINH T

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/15/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/921,561	KOMURA ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- Th MAILING DATE of this communication app ars on th cov r sh et with th correspond nce address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-31 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-31 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 06 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claims 2, 5-9, 18-19, 22-23, 28-29 and 31 are objected to because of the following informalities:

As per claim 2, --the-- should be inserted on line 5 before --selecting switch sections--.

As per claim 5, "output terminal side" recited on line 2 should be changed to --the output terminals-- since it is used to refer to the output terminals recited on lines 7-8 of claim 4.

As per claim 6, "an" recited on line 3 should be changed to --the--.

As per claim 7, --the-- should be inserted after "between' recited on line 8 since the term "output terminals" already recited on lines 7-8 of claim 4.

As per claim 8, "an output terminal side" should be changed to --the output terminals-- since it is used to refer to the output terminals recited on lines 7-8 of claim 4. The phrase "first power supply voltage side" recited on line 4 and the phrase --second power supply voltage side" should be changed to --first power supply voltage-- and --second power supply voltage--, respectively.

As per claim 9, the same problems exist for the "output terminal side" recited on line 2, "the first power supply voltage side" recited on line 4 and "the second power supply side" recited on line 5 as discussed in claim 8.

As per claim 18, "an" recited on line 3 should be changed to --the-- since the term "input signal" is already recited on line 3 of claim 1.

As per claim 19, "wherein the predetermined delay stages are formed" recited on lines 1-2 should be changed to --wherein each of the predetermined delay stages is formed--. "an" recited on line 4 should be changed to --the--.

As per claim 22, "the" recited on line 4 should be changed to --a-- to avoid potential antecedent basis problem.

As per claim 23, "the" recited on line 4 should be deleted.

As per claim 28, "an" recited on line 3 should be changed to --the-- since the term "input signal" is already recited on line 3 of claim 26.

As per claim 29, the phrase "each predetermined delay time" recited on lines 4-5 should be changed to --each of the predetermined delay times" to be consistent with the recited "predetermined delay times" recited on line 2. "the", first occurrence, recited on line 7 should be changed to --a--.

As per claim 31, "the predetermined delay times have" recited on line 2 should be changed to --each of the predetermined delay times has--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, the phrase "for combining the predetermined delay stages as appropriate" recited on lines 4-5 is indefinite because it fails to particularly point out the combination of the delay section and the selecting switch sections which are considered appropriate, i.e., the claim must recite a structural relationship between the delay stages and the selecting switch sections which is deemed to be appropriate. The recitation on the last five lines are indefinite because it is unclear whether the recitation means each of the selecting switch sections has a buffer section and a selecting section or each of the selecting switch sections has a plurality of buffer sections and a plurality of selecting sections or else. For further examination, it is assumed that each selecting switch section comprises a buffer section and a selecting section.

As per claim 2, the term "the predetermined delay times" lacks clear antecedent basis, i.e., it is not clear if it this is referring to the "predetermined delay time" recited on line 3 of claim 1.

As per claim 3, the same problem exists for the recited "predetermined delay times" recited on line 4 as discussed in claim 2. The recited limitation "the rise delay time and fall delay time for the input signals are balanced" on lines 4-5 is not clear, i.e., it is not clear if the recitation means the delay times of the rise time and the fall time are the same. For further examination, it is assumed that the recitation means the delay times of the rise time and fall time are the same.

As per claim 18, the recited limitation "the rise delay time and fall delay time for an input signals are balanced" on lines 2-3 is not clear, i.e., it is not clear if the recitation means the delay times of the rise time and the fall time are the same.

As per claim 19, the recited limitation "the rise delay time and fall delay time for an input signals are balanced" on lines 4-5 is not clear, i.e., it is not clear if the recitation means the delay times of the rise time and the fall time are the same.

As per claims 1-25, these claims are rejected because of the indefiniteness of claim 1.

As per claim 21, the claim is indefinite because the limitation "the rise delay time and fall delay time of an input signal are different" recited on lines 4-5 is conflict with the limitation recited in claim 18, i.e., "the rise delay time and fall delay time for an input signal are balanced" which means they are the same.

As per claim 25, the recitation " transistors series having the same functions as the second or fourth transistors" on lines 4-5 is indefinite because the recitation fails to particularly point out a structure which has more than two transistors and performs the same function as one transistor as recited.

As per claim 26, the recitation that the semiconductor integrated circuit device comprises selection switch sections, buffer sections and selecting sections is misdescriptive because the buffer sections and the selecting sections are part of the selecting switch sections. The phrase "combine the predetermined delay stages as appropriate" recited on lines 9-10 is indefinite for the reasons noted in claim 1 above. The term "a delay path" recited on lines 10-11 lacks clear antecedent basis, i.e., it is not clear if it is referring to the delay path recited on line 7. The term " the desired delay time" recited on line 12 lacks antecedent basis.

As per claim 28, , the recited limitation "the rise delay time and fall delay time for an input signals are balanced" on lines 2-3 is not clear, i.e., it is not clear if the recitation means the delay times of the rise time and the fall time are the same.

As per claims 27-28, these claims are rejected because of the indefiniteness of claim 26.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4, 6-7, 9-13, 16-18 and 25-31 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,521,540 to Marbot.

As per claim 1, Marbot discloses a delay circuit (Fig. 7) comprising:

a delay section having two or more predetermined delay stages (delay stages D1, D2, ..., D4) in which a predetermined delay time (the total delay time D1+D2+D3+ ...) is added to an input signal E0; and

selecting switch sections (U0, U1, ..., U4) for combining the predetermined stages as appropriate (the combination shown) and establishing a delay path (the path from E0 to Fk that outputs a delayed output signal) having the desired delay time; wherein

each of the selecting switch sections (U1, for example) comprises:

a buffer section (transistors P1 and N1) for inputting propagated signal E1 from the input signal E0;

a selecting section (transistors SW1* and SW1) for activating the buffer section when the delay path is being established in the delay section.

As per claim 2, Marbot further discloses:

in the delay section, the predetermined delay stages (D1, D2, ..., D4) are provided with individual delayed output terminals (E1, ..., E4) for outputting individual delayed output signals (the signals at E1,... , E4);

the selecting switch sections (U1, ..., U4) are provided for each individual delayed output terminals (E0, ..., E4) with input terminals of the buffer sections (P1,N1; ..., P4,N4) being connected to the individual delayed output terminals and output terminals of the selecting switch sections being mutually joined (connected to line L).

As per claim 3, Marbot further discloses:

in the delay section, the predetermined delay stages (D1, D2, ..., D4) are provided with individual delayed input terminals (E0, ..., E3) for inputting signals (the signals at E0,... , E3) to which predetermined delay times are added, the rise delay time and fall delay time for the input signal of each of the delay stages in the Marbot are balanced because the Marbot circuit has the same structure of the recited delay circuit structure; and

the selecting switch sections (U0, ..., U4) are provided for each individual delayed input terminals (E0, ..., E3) with input terminals of the buffer sections (P0,N0; ..., P4,N4) being connected to the individual delayed input terminals and the input terminals of the selecting switch sections being mutually joined (connected to line L).

As per claim 4, the recited first transistors read on transistors (P0, ..., P4) having gate terminals set as input terminals, the recited second transistors read on transistors (SW*0, ..., SW*4) whose gate terminals control signals (A0, ..., A4) for establishing the delay path, and the first and second transistors are connected in series between the output terminals (line L) and a first power supply voltage VDD.

As per claim 6, as shown in Fig. 7, the first transistors (P0, ..., P4) are provided at the first power supply side VDD and the second transistors (SW*0, ..., SW*4) are provided at the output terminal side of the selecting switch sections.

As per claim 7, the recited third transistors read on transistors (N0, ..., N4), the recited fourth transistors read on transistors (SW0, ..., SW4), the recited second power supply voltage reads on the supply voltage VSS. These elements are connected as recited.

As per claim 9, Fig. 7 shows the first, second, third and fourth transistors are connected as recited in the claim.

As per claim 10, the first power supply voltage VDD is the recited power supply voltage potential, and Fig. 8 shows the first and second transistors are PMOS transistors.

As per claim 13, the second power supply voltage VSS is the recited ground supply voltage potential, and Fig. 8 shows the third and fourth transistors are NMOS transistors.

As per claims 11 and 12, these claims are merely the same as claims 10 and 13, respectively when the names of the first and second transistors are interchanged with the names of the third and fourth transistors and the names of the first and second power supply voltages are interchanged, and therefore, they are rejected for the same reasons as discussed in claim 10 and 13.

As per claim 16, the recited connections of the delay stages are shown in Fig. 7.

As per claim 17, this claim is rejected for the same reason noted in claim 16.

As per claim 18, since the recited predetermined delay stages do not have any structural different from the Marbot's predetermined delay stages, they should output the same results, i.e.,

the rise delay time and fall delay time for an input signal are also balanced so as to be substantial uniform.

As per claim 25, as shown in Fig. 8, more controls (K0, K*0) and more transistors (the transistors which receives control signals K0, K*0) are added in series.

As per claim 26, this claim is rejected for the same reason noted in claim 1.

As per claims 27-28, these claims are rejected for the same reasons noted in claims 4 and 18, respectively.

As per claim 29, this claim is merely a method to operate the delay circuit having elements and connections as discussed in claim 1 above, since Marbot teaches the circuit, he inherently teaches the method wherein the recited delay step is performed by delays D1, ...,D4; the recited output step is the result signals at output nodes of the delay stages D1, ..., D4; and the recited selecting step is performed by control signals (A0, ..., A4) via switches (SW0, ..., SW4).

As per claim 30, the recited required power reads on the power supply VDD.

As per claim 31, this claim is rejected for the same reason noted in claim 18.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5, 8, 14-15 and 19-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,521,540 to Marbot.

As per claim 5, Marbot teaches a delay circuit as discussed in claim 4 above wherein the first transistors are provided at the first power supply side VDD and the second transistors are provided at the output terminal side (line L) and these transistors are in series but he does not explicitly teach that these transistors can be interchanged, i.e., the first transistors are provided at the output terminal side (line L) and the second transistors are provided at the first power supply side VDD.

However, it is notoriously well-known to a person skilled in the art that the position of these transistors can be interchanged since in either location they perform the same function and output the same results. Since they are art recognized equivalent, during assembly process, the worker can perform the rearrangement so that the layout yields the most convenient way to receive the control signals and input signals and /or further minimize the electromagnetic interference problems (EMI).

It would have been obvious to one skilled in the art at the time of the invention was made to provide the second transistors (SW*0, ..., SW*4) at the first power supply side VDD and the first transistors (P0, ..., P4) at the output side in the Marbot's delay circuit.

The motivation/suggestion for doing so would have been obvious for the reasons discussed herein above.

Therefore, it would have been obvious to interchanged to locations of the first and second transistors in the Marbot delay circuit to obtain the invention specified in the claim.

As per claim 8, Marbot teaches a delay circuit as discussed in claim 7 above wherein the first transistors are provided at the first power supply side VDD, the second and fourth transistors are provided at the output terminal side (line L), and the third transistors are provided at the

second power supply side VSS but he does not explicitly teach that the second transistors are provided at the first power supply side VDD, the first and third transistors are provided at the output terminal side (line L), and the fourth transistors are provided at the second power supply side VSS as called for in the claim.

However, the recited arrangement is an obvious alternation of the arrangement shown in Fig. 7 of the Marbot reference, and one skilled in the art would be motivated to rearrange the transistors in the Marbot circuit to be the same as the one recited in the claim for the reasons and motivations discussed in claim 5 above.

As per claim 14, Marbot teaches a delay circuit as discussed in claim 4 above wherein the first transistors which are functioned as buffers are provided at the first power supply side VDD and the second transistors which are functioned as switches are provided at the output terminal side (line L) but he does not explicitly disclose that the drive capacity of the second transistors are larger than the drive capacity of the first transistors as called for in the claim.

However, it is notoriously well-known to a person skilled in the art that a transistor which is functioned as a switch introduces a delay when a signal passes through, and by increasing the drive capacity of the transistor, the delay caused by the transistor is reduced.

It would have been obvious to one skilled in the art at the time of the invention was made to use a larger drive capacity of the second transistors than the drive capacity of the first transistors in the Marbot delay circuit.

The motivation/suggestion for doing so would have been to improve the accuracy of the Marbot delay circuit by eliminating the unaccounted delays by the switches.

Therefore, it would have been obvious to use the second transistors having drive capacity larger than the drive capacity of the first transistors in the Marbot delay circuit to obtain the invention specified in the claim.

As per claim 15, this claim is rejected for the same reason and motivation as discussed in claim 14.

As per claim 19, Marbot discloses the delay circuit which includes predetermined delay stages D1, ..., D4 as discussed in claim 18 above but he does not explicitly disclose that each of the delay stages is implemented using even basis units connected in series as called for in the claim.

The examiner takes Official Notice that it is old and well-known in the art to use inverters connected in series as a delay stage, and each of the inverters is counted as a basis unit delay, two inverters can be connected in series to implement a delay stage in a delay circuit so that the rise and fall times of an input signal are balanced.

It would have been obvious to one skilled in the art at the time of the invention was made to use two inverters connected in series to implement each of the Marbot's delay stages D1, ..., D4.

The motivation/suggestion for doing so would have to obtain a balanced rise and fall time of the output signal when the signal is delayed by the Marbot's delay circuit.

Therefore, it would have been obvious to use two inverters to implement each of the Marbot delay stages to obtain the invention specified in the claim.

As per claim 20, the modification discussed in claim 19 clearly discloses the logic inversion sections are inverter gates.

As per claim 21, this claim is rejected for the same reasons noted in claim 19. Regarding the limitation that the rise delay time and fall delay time of an input signal are different, this limitation is met when the delay stage is implemented using odd number of inverters.

As per claim 24, Marbot discloses the delay circuit which includes predetermined delay stages D1, ..., D4 as discussed in claim 16 above but he does not explicitly disclose that each of the delay stages having the same structure.

The examiner takes Official Notice that using the same structure to implement each of the delay stages has the advantage of cost reducing since they are able to mass production.

It would have been obvious to one skilled in the art at the time of the invention was made to implement the Marbot delay stages using the same structure for the advantage of minimizing the cost.

As per claims 22 and 23, the combination discussed in claim 21 above discloses the delay circuit includes predetermined delay stages D1, ..., D4 wherein each of the delay stage is implemented using two inverters connected in series but he does not explicitly disclose that each of the delay stages is implemented using NAND gates to function as inverters by connecting one of its input terminal to VDD as called for in claim 22 or each of the delay stages is implemented using NOR gates to function as inverters by connecting one of its input terminal to ground as called for in claim 23.

The examiner takes Official Notice that an NAND gate with one of its input terminals connected to VDD or a NOR gate with one of its input terminals connected to ground is art recognized equivalent to an inverter since it is functioned as an inverter.

It would have been obvious to replace the inverters used to implement the delay stages in the combination discussed in claim 21 with NAND gates or NOR gates.

The suggestion/motivation for doing so would have been obvious since during the assembly process of the Marbot circuit, a worker would be motivated to replace the inverter in the Marbot delay stage by a NAND gate or NOR gate when the inverter is not readily available, and therefore, time for waiting the parts is saved.

Therefore, it would have been obvious to replace the inverters in the delay stage of the Marbot circuit by NOR gates as called for in claim 23 or by NAND gates as called for in claim 22 to obtain the invention specified in the claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent No. 6,175,605 to Chi discloses a delay circuit (Fig. 3a) which includes a plurality of delay stages wherein each delay stage includes two inverters and control stages for each of the corresponding delay stages.

US Patent No. 5,355,037 discloses a delay circuit (Fig. 3) which includes a plurality of delay stages (33, 35) wherein each delay stage includes two inverters (33, 35) and control stages for each of the corresponding delay stages.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is 703-306-9179. The examiner can normally be reached on Monday - Thursday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 703-308-4876. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Minh Nguyen
Examiner
Art Unit 2816

January 8, 2002